REMARKS

Claims 1-27 are pending in this Application No. 10/608,864 by Pang, et. al. ("Pang").

Claim Rejections Under 35 USC §102(e):

Claims 1-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Levine et. al. US Patent No. 5,835,702 ("Levine"). Applicants respectfully traverse the rejection of claims 1-27. Reconsideration and withdrawal of these rejections is respectfully requested in light of the remarks provided below.

In order for a claim to be anticipated under § 102, the anticipating reference must disclose at least one embodiment that incorporates all of the claimed elements. See, for example, C.R. Bard, Inc. v. M3 Systems, 48 U.S.P.Q.2d 1225, 1230 (Fed. Cir. 1998) ("When the defense of lack of novelty is based on a printed publication that is asserted to describe the same invention, a finding of anticipation requires that the publication describe all of the elements of the claims, arranged as in the patented device..."); In re Bond, 15 U.S.P.Q2d 1566, 1567 (Fed. Cir. 1990) ("For a prior art reference to anticipate in terms of 35 U.S.C. § 102, every element of the claimed invention must be identically shown in a single reference..."). So, in order for the above claims to be anticipated by Levine, Levine must contain every element in claims 1-27.

Contrast of Levine and Pang

Levine discloses a performance monitor 50 shown in Figure 4 of Levine. This performance monitor includes a number of performance monitor counters ("PCM") 51 that are used to count processor/storage events. Associated with the PCMs are monitor mode control registers ("MMCR"), with each MMCR controlling a number of PCMs. The description of this architecture is found in Levine, col 7 and 8.

Note that in Levine, Figure 4, the performance monitor 50 is clearly labeled as being implemented in the **hardware** of the processor 10 of Figure 1. A careful reading by one skilled in the art of the description of the performance monitor in the remainder of columns 7 and 8 verifies that the performance monitor of Levine operates through hardware instructions,

e.g., Levine, col. 8 lines 39-40: "The PM 50 then saves the machine state values in special purpose registers," and col. 8 lines 63-65: "When the PM 50 receives notification from the time base 52... an interrupt signal is output to a branch processing unit 20."

The pending application, however, teaches towards a performance monitor system implemented not in hardware, but at the **application level of the software**. This is clearly stated in several places of the application, for example, in Pang, page 2, lines 18-21: "The performance counter provider for an application containing performance counters, consists of software written specifically for the particular application with which it is associated," and in Pang, page 6, lines 26-29: "Before turning to the figures, it is noted that in an embodiment of the present invention computers implement steps described herein by executing software instructions, such as program modules." The software implementation is also shown by the illustration of the interaction between the operating system and the application processes in Pang, Figure 3, and the illustrations of exemplary data structures and application program function software implementations in Pang, Figures 4-6.

The uses of the term "function" in the dependent claims and "application program interface" in the independent claims signify a software implementation to one skilled in the art, or to even to one with access to Wikepedia's common language understanding:

> An **application programming interface** (API) is a source code interface that a computer system or program library provides to support requests for services to be made of it by a computer program. An API differs from an application binary interface in that it is specified in terms of a programming language that can be compiled when an application is built, rather than an explicit low level description of how data is laid out in memory.

To further amplify this distinction in the claims, the independent claims 1, 9, 17, 25, 26 and 27 and their associated dependent claims 2, 5, 10, 13, 18 and 21 are amended to consistently use the term "application process" to more distinctly emphasize the implementation at the software application process level and not the hardware level. Levine does not teach an embodiment where the elements of performance counter consumer application processes and performance counter provider application processes are implemented at the software application level, therefore the 35 USC §102(e) rejection does not apply.

Remarks regarding the cited referenced sections

Levine, col. 2, lines 51-64 refers to the hardware performance monitor of Figure 3 and cols. 7-8, which is not a software embodiment of a performance counter consumer application process, a performance counter provider application process, and an application program interface comprising a set of software functions.

Levine, col. 9, lines 32-55 refers to performance monitoring routines performed by the hardware performance monitor of Levine, Figure 4, as stated in the preamble to this section col. 9, lines 13-15: "... performance monitoring is implemented... through configuration counters by the monitor mode control registers...."

Levine, col. 9, lines 17-25 refers to the same hardware performance monitor of Figure 4, as stated in col. 9, lines 13-15.

Levine, col. 10, lines 7-16 refers to a monitor mode control register (MMCR0) controlling the operation of two performance monitor counters of the same hardware performance monitor of Figure 4 (see col. 9, 56-58).

Levine, col. 7, lines 35-47 directly defines the architecture of the hardware performance monitor 50.

Levine, col. 4, lines 24-36 refers to the operation of a load/store unit in a processor that does not encompass an embodiment at a software level of a performance counter consumer application process, a performance counter provider application process, and an application program interface comprising a set of software functions.

Levine, col. 6, lines 21-31 refers to the operation of a sequencer unit and dispatch logic which are executed at a lower level than software, and are not an embodiment at a software level of a performance counter consumer application process, a performance counter provider application process, and an application program interface comprising a set of software functions.

Levine, col. 4, lines 64-67 – col. 5, lines 1-9 also refer to the sequence unit and rename buffers which are executed at a lower level than software application processes.

None of the cited references teach an embodiment disclosed in the independent claims of Pang, where the elements of performance counter consumer application processes and performance counter provider application processes are implemented at the software application level. Levine does not teach every element of Pang and the 35 USC §102(e) rejection does not apply.

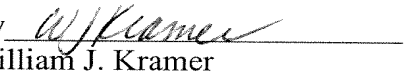
CONCLUSION

In view of the above amendment and arguments, the applicant submits the pending application is in condition for allowance and an early action so indicating is respectfully requested.

The Commissioner is authorized to charge any fee deficiency required by this paper, or credit any overpayment, to Deposit Account No. 13-2855, under Order No. 30835/302623, from which the undersigned is authorized to draw.

Dated: June 11, 2007

Respectfully submitted,

By 

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